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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,995	12/30/2003	Hong-Jyh Li	2003 P 54309 US	8237

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EXAMINER	
KANG, DONGHEE	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,995	LI, HONG-JYH	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 33-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-8* is/are allowed.

6)☒ Claim(s) *9-10,15-16, 33-34,& 36-39* is/are rejected.

7)☒ Claim(s) *11-14,35, & 40-44,* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field April 21, 2005.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims **15 & 38** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

the phrase "forming isolation regions in the workpiece, before or after forming the stressed semiconductor layer" is not supported by the specification. The embodiment figs. 6-8 including a stressed semiconductor layer (422 or 522) do not show the isolation regions (404 & 504) formed in the workpiece (402 or 516) but in the stressed semiconductor layer.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim **39** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 39 recites the limitation "in the stressed semiconductor layer" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Objections

6. Claim **40** is objected to because of the following informalities: The phrase "stressed semiconductor layer" in lines 11-12 should be - -the layer of semiconductor material- - because there is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims **9-10 & 36** are rejected under 35 U.S.C. 102(b) as being anticipated by Candelaria (US 5,683,934).

Re claim 9, Candelaria teaches a method of fabricating a transistor, the method comprising (Fig.3):

providing a workpiece (11); forming a first layer of silicon and carbon (12) over the workpiece; depositing a gate dielectric material (17) directly on the layer of silicon

and carbon, depositing a gate material (18) over the gate dielectric material; patterning the gate material and gate dielectric material to form a gate and a gate dielectric disposed over the layer of silicon and carbon (Col.4, lines 31-37); and forming a source region and drain region in at least the layer of silicon and carbon wherein the source region, drain region, gate, and gate dielectric comprise a transistor.

Re claim 10, Candelaria teaches forming the layer of silicon and carbon comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10% carbon having a thickness of about a few tens of Å to about 5 μm. See Col.3, lines 51-57.

Re claim 36, Candelaria teaches forming a first layer of silicon and carbon over the workpiece comprises growing a first layer of silicon and carbon over the workpiece.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims **16 & 37** are rejected under 35 U.S.C. 103(a) as being unpatentable over Candelaria (US 5,683,934) in view of Yu et al. (US 6,784,101).

Re claim 16, Candelaria does not teach forming spacers over sidewalls of the gate and gate dielectric.

Yu teaches forming spacer (10, Fig.6) over sidewalls of the gate and gate dielectric to provide a protection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form spacers over sidewalls of the gate and gate dielectric to provide a protection as taught by Yu in Candelaria's method in order to provide a protection for gate electrode from environmental damages.

Re claim 37, Candelaria does not teach the workpiece comprises providing a silicon-on-insulator (SOI) wafer. Yu teaches forming transistor on Si wafer or SOI substrate (Col.6, lines 56-57). It is well known in the art that SOI technology allows the formation of high-speed, shallow-junction device. In addition, SOI improves performance by reducing parasitic junction capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor on SOI substrate since SOI improves performance of transistor by reducing parasitic junction capacitance.

11. Claims **9-10, 33-34, & 36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo et al. (US 2003/0102490) in view of Yu (6,784,101)

Re claim 9, Kubo et al. teach a method of fabricating a transistor, the method comprising (Fig.1):

providing a workpiece (10); forming a first layer of silicon and carbon (12) over the workpiece; depositing a gate dielectric material (13) directly on the layer of silicon and carbon, depositing a gate material (14) over the gate dielectric material; forming a

gate and a gate dielectric disposed over the layer of silicon and carbon; and forming a source region and drain region in at least the layer of silicon and carbon wherein the source region, drain region, gate, and gate dielectric comprise a transistor. Kubo et al. do not explicillty teach patterning step to form gate dielectric layer and gate electrode. It is conventional in the art and Yu et al. also teach patterning step to form gate dielectric layer and gate electrode. Therefor, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform patterning step as taught by Yu in Kubo's method since it is a known method well suited for the intended purpose.

Re claim 10, Kubo et al. teach forming the layer of silicon and carbon comprises epitaxially growing a layer of about 90 to 99.5% silicon and about 0.5 to 10% carbon having a thickness of about a few tens of Å to about 5 μm.

Re claim 33, Kubo et al. teach the gate dielectric comprising a high dielectric constant material.

Re claim 34, Kubo et al. teach depositing a gate material over the gate dielectric material comprises depositing a gate material that comprises a metal.

Re claim 36, Kubo et al. teach forming a first layer of silicon and carbon over the workpiece comprises growing a first layer of silicon and carbon over the workpiece.

Allowable Subject Matter

12. Claims 1-8 are allowed.

13. Claims 13-14 & 40-44 would be allowable if rewritten or amended to overcome objection, set forth in this Office action.

Response to Arguments

14. Applicant's arguments with respect to claim 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang
Primary Examiner
Art Unit 2811

dhk